Notice of Allowability	Application No.	Applicant(s)
	10/734,296	YAMASAKI ET AL.
	Examiner	Art Unit
	Connie C. Yoha	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/25/05*.

2. ☒ The allowed claim(s) is/are *1-32*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

DETAILED ACTION

Response to Arguments

1. Examiner took notice of the remarks and amendments made by applicant filed on 10/25/05.

Response to Amendment

2. This office action is in response to Amendment filed on 10/25/05.

3. Claims 1-32 are pending.

Allowable Subject Matter

4. Claims 1-32 are allowed.

5. Claims 1-32 are considered allowable since prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations having in combination with other features, a memory device having memory cell including an access transistor of an MISFET, wherein a positive power supply voltage is applied to the first bit line in a high level state and a ground voltage is applied to the first bitline in a low level state, wherein the access transistor is a depletion type p-channel MISFET, and wherein the ground voltage is applied to a gate electrode of the access transistor through the word line when the memory cell is in an activated state.

Prior art also does not disclose an integrated circuit having in combination with other features, a logic circuit which includes a p-channel MISFET and is integrated on a substrate; and a dynamic memory device provided on the substrate on which the logic circuit is provided, a memory cell including an access transistor of a p-channel MISFET,

wherein the threshold voltage of the access transistor is set to be higher than that of the p-channel MISFET provided in the logic circuit.

Prior art also does not disclose an integrated circuit having in combination with other features, a logic circuit which includes a n-channel MISFET and is integrated on a substrate; and a dynamic memory device provided on the substrate on which the logic circuit is provided, a memory cell including an access transistor of a n-channel MISFET, wherein the threshold voltage of the access transistor is set to be lower than that of the n-channel MISFET provided in the logic circuit.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, Amir Zarabian, can be reached at (571) 272-1852. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you

have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.Yoha

December 2005

CONNIE C. YOHA
PRIMARY EXAMINER